CLAIMS

What is claimed is:

1. A wafer-level chip scale package, comprising:

a chip pad over a substrate;

a re-distributed line (RDL) pattern on the chip pad; and

an insulating layer covering a portion of the RDL pattern, wherein the insulating layer comprises a non-polymeric dielectric material.

2. The package of claim 1, further comprising a stud bump on the portion of the RDL pattern not covered by the insulating layer.

3. The package of claim 2, further comprising a solder ball on the stud bump.

4. The package of claim 1, further comprising a passivation layer between the substrate and the RDL pattern.

5. The package of claim 1, wherein the substrate contains an integrated circuit in communication with the chip pad.

6. The package of claim 1, wherein the insulating layer comprises silicon nitride, silicon oxide, or silicon oxynitride.

7. The package of claim 1, wherein the chip pad and the RDL pattern comprise aluminum.

8. The package of claim 2, wherein the stud bump comprises Cu.

9. The package of claim 8, wherein the stud bump is a coined stud bump.

10. The package of claim 2, wherein there is no under bump metal between the chip pad and the RDL pattern.

11. A wafer-level chip scale package, comprising:

a chip pad over a substrate;

a re-distributed line (RDL) pattern on the chip pad;

an insulating layer covering a portion of the RDL pattern, wherein the insulating layer comprises a non-polymeric dielectric material; and

a stud bump on the portion of the RDL pattern not covered by the insulating layer.

12. The package of claim 11, further comprising a solder ball on the stud bump.

13. The package of claim 11, wherein the insulating layer comprises silicon nitride, silicon oxide, or silicon oxynitride.

14. The package of claim 11, wherein there is no under bump metal between the chip pad and the RDL pattern.

15. A packaged semiconductor device, comprising:

a chip pad over a substrate;

a re-distributed line (RDL) pattern on the chip pad;

an insulating layer covering a portion of the RDL pattern, wherein the insulating layer comprises a non-polymeric dielectric material; and

a stud bump on the portion of the RDL pattern not covered by the insulating layer.

16. The device of claim 15, further comprising a solder ball on the stud bump.

17. The device of claim 15, wherein the insulating layer comprises silicon nitride, silicon oxide, or silicon oxynitride.

18. The device of claim 15, wherein there is no under bump metal between the chip pad and the RDL pattern.

19. An electronic apparatus containing a packaged semiconductor device, the device comprising:

a chip pad over a substrate;

a re-distributed line (RDL) pattern on the chip pad;

an insulating layer covering a portion of the RDL pattern, wherein the insulating layer comprises a non-polymeric dielectric material; and

a stud bump on the portion of the RDL pattern not covered by the insulating layer.

20. A method for making wafer-level chip scale package, comprising:

providing a chip pad over a substrate;

providing a re-distributed line (RDL) pattern on the chip pad;

providing an insulating layer covering a portion of the RDL pattern, wherein the insulating layer comprises a non-polymeric dielectric material; and

providing a stud bump on the portion of the RDL pattern not covered by the insulating layer.

21. The method of claim 20, further comprising providing a solder ball on the stud bump.

22. The method of claim 20, wherein the insulating layer comprises silicon nitride, silicon oxide, or silicon oxynitride.

23. The method of claim 20, wherein there is no under bump metal between the chip pad and the RDL pattern.

24. A method for making wafer-level chip scale package, comprising:

providing a substrate with a passivation layer on a portion thereof;

forming a chip pad on a portion of the substrate not containing the passivation layer;

forming a metal layer on the chip pad and a portion of the passivation layer;

forming an insulating layer on a portion of the RDL pattern, wherein the insulating layer comprises a non-polymeric dielectric material; and

forming a stud bump on the portion of the RDL pattern not covered by the insulating layer.

25. The method of claim 24, further comprising providing a solder ball on the stud bump.

26. The method of claim 24, wherein the insulating layer comprises silicon nitride, silicon oxide, or silicon oxynitride.

27. The method of claim 24, including forming the insulating layer without using a high temperature curing process.

28. The method of claim 24, wherein there is no under bump metal between the chip pad and the RDL pattern.

29. The method of claim 24, including forming the stud bump by an electroplating process or by wire bonding.

30. The method of claim 29, including forming the stud bump by wire bonding a Pd coated copper wire to the RDL pattern using a capillary.

31. The method of claim 30, wherein the wire bonding process provides the stud bump with a coined shape.

32. A method for making a package semiconductor device, comprising:

providing a chip pad over a substrate;

providing a re-distributed line (RDL) pattern on the chip pad;

providing an insulating layer covering a portion of the RDL pattern, wherein the insulating layer comprises a non-polymeric dielectric material; and

providing a stud bump on the portion of the RDL pattern not covered by the insulating layer.

33. A method for making an electronic apparatus containing a packaged semiconductor device, the method comprising:

providing a packaged semiconductor device containing a chip pad over a substrate, a re-distributed line (RDL) pattern on the chip pad, an insulating layer covering a portion of the RDL pattern with the insulating layer comprising a non-polymeric dielectric material, and then providing a stud bump on the portion of the RDL pattern not covered by the insulating layer; and

mounting the packaged semiconductor device on a circuit board.